Abstract: An event-based image sensor comprising a plurality of pixel circuits (1) each comprising: a photoreceptor circuit (10) comprising a light-sensitive element (101) configured for delivering at an output (11) a photoreceptor current (IpRon), an analog bus (20), a bank of current memory cells connected to the analog bus (20), each adapted to store an electric current flowing in the analog bus (20) and to deliver an electric current stored within said current memory cell, wherein each pixel circuit (1) comprises a current comparator (50) comprising: a current sign detector (51) connected to the analog bus (20) and configured for comparing a value of a compared electric current resulting from a difference between the photoreceptor current and a previous photoreceptor current stored in a current memory cell, at least one storage cell (53, 54) having a state conditioned by the output of said current sign detector (51).
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EVENT-BASED IMAGE SENSOR AND OPERATING METHOD THEREOF

CONTEXT AND BACKGROUND OF THE INVENTION

The invention relates to an event-based image sensor and an operating method thereof.

Conventional image sensors acquire the visual information time-quantized at a predetermined frame rate. Each frame carries the information from all pixels, regardless of whether or not this information has changed since the last frame has been acquired. This approach obviously results, depending on the dynamic contents of the scene, in a more or less high degree of redundancy in the recorded image data. The problem worsens as modem image sensors advance to ever higher spatial and temporal resolution. The hardware required for post-processing of the data increases in complexity and cost, demand on transmission bandwidth and data storage capacity surges and the power consumption rises, leading to severe limitations in all kinds of vision applications, from demanding high-speed industrial vision systems to mobile, battery-powered consumer devices.

One approach to dealing with temporal redundancy in video data is frame difference encoding. This simplest form of video compression includes transmitting only pixel values that exceed a defined intensity change threshold from frame to frame after an initial key-frame. Known frame differencing imagers rely on acquisition and processing of full frames of image data and are not able to self-consistently suppress temporal redundancy and provide real-time compressed video output. Furthermore, even when the processing and difference quantization is done at the pixel-level, the temporal resolution of the acquisition of the scene dynamics, as in all frame-based imaging devices, is still limited to the achievable frame rate and is time-quantized to this frame rate.

The adverse effects of data redundancy are most effectively avoided by not recording the redundant data in the first place and directly reducing data volume at the sensor output level. The immediate benefits are reductions in bandwidth, memory and computing power requirements for data transmission and post-processing, hence decreasing system power, complexity and cost. In addition, the frame-based, clocked principle of operation of conventional CMOS or CCD image sensors leads to limitations in
temporal resolution as scene dynamics are quantized to the frame rate at which the pixel field of view is readout, and poor dynamic range.

The problem to be solved by the present invention is to provide an image sensor and the operating method thereof for the continuous acquisition of the full visual information of an observed dynamic scene with high temporal and intensity resolution, over a wide dynamic range (of recordable and processable light intensity) and thereby generating the minimum necessary amount of data volume. Thus, the generated data are not constituted by a succession of frames containing the image information of all pixels, but a stream of change and intensity (i.e. grey level) information of individual pixels, which are recorded and transmitted only if an actual change in light intensity in the field of view of the individual pixel has been detected by the pixel itself.

This method leads to a substantial reduction of generated data through complete suppression of the temporal redundancy in the picture information that is typical for conventional image sensors, though with the data containing the same, or even higher, information content. The picture element for an image sensor that implements the aforementioned method as well as the required asynchronous data readout mechanism can be realized on basis of electronic circuits. An image sensor with a multiplicity of such picture elements is typically realized and fabricated as an integrated system-on-chip e.g. in CMOS technology.

Implementing such a sensor and thus avoiding the above mentioned drawbacks of conventional image data acquisition would be beneficial for a wide range of artificial vision applications including industrial high-speed vision (e.g. fast object recognition, motion detection and analysis, object tracking, etc.), automotive (e.g. real-time 3D stereo vision for collision warning and avoidance, intelligent rear-view mirrors, etc.), surveillance and security (scene surveillance) or robotics (autonomous navigation, SLAM) as well as biomedical and scientific imaging applications. As the sensor operation is inspired by working principles of the human retina, one advantageous example application is the treatment of a degenerated retina of a blind patient with an implantable prosthesis device based on the data delivered by such a sensor.

A solution for achieving the aforementioned complete temporal redundancy suppression is based on pixel-individual pre-processing and acquiring of the image information, event-controlled and conditionally (i.e. only when changes in the scene have
been detected). As explained below, the control of the image data acquisition is transferred to the pixel-level.

An electronic circuit, often call a transient detector, is used for detecting changes in lighting intensity received by the individual, autonomously operating pixels, for example in the case of an optical transient sensor, or dynamic vision sensor (DVS), as described in patent US 7,728,269. However, such a transient detector circuit requires large switched-capacitors, and mismatch between voltage comparators used for assessing the changes may be problematic.

Patent US 8,780,240 discloses combining transient detector circuits, i.e. light exposure intensity changes detector circuits, and conditional exposure measurement circuits. A transient detector circuit individually and asynchronously initiates the measurement of a new exposure measure only if - and immediately after - a brightness change of a certain magnitude has been detected in the field-of-view of a pixel. Such a pixel does not rely on external timing signals and independently requests access to an (asynchronous and arbitrated) output channel only when it has a new grayscale value to communicate. Consequently, a pixel that is not stimulated visually does not produce output. In addition, the asynchronous operation avoids the time quantization of frame-based acquisition and scanning readout.

For each pixel circuit, the transient detector circuit monitors a photoreceptor voltage derived from a first photodiode for detecting relative voltage changes that exceed a threshold. Upon such detection, the transient detector circuit outputs a command for the exposure measurement circuit of the same pixel to start an absolute intensity measurement, i.e. an absolute grey level measurement. The exposure measurement circuit uses a second photodiode of the pixel, placed adjacent to the first photodiode, and derives its measure from the time duration for discharging the photodiode junction capacitance with the instantaneous photocurrent.

However, the pixel circuit disclosed in US 8,780,240 is not optimal since time-based exposure measurement through direct photocurrent integration is only available after an unknown integration time. Furthermore, it often leads to a prohibitively long measurement time of a new exposure value, especially at low pixel illuminance levels, due to the corresponding small photocurrents. Finally using two separate photodiodes for change detection and exposure measurement leads to spatial divergence and motion
direction dependency of the image data acquisition process, resulting in a reduction in imaging quality.

Patent application US 2016/0227135 A1 discloses a pixel circuit comprising:

- a front-end circuit comprising a single photodiode and having an output, said front-end circuit being configured for delivering on said output a photoreceptor signal derived from a light exposure of said photodiode;
- a transient detector circuit configured for detecting a change in said photoreceptor signal delivered on said output;
- an exposure measurement circuit configured for measuring said photoreceptor signal delivered on said output upon detection by the transient detector circuit of a change in the photoreceptor signal, said exposure measurement circuit having a capacitor connected by a first switch to the output of the front-end circuit.

However, the exposure measurement is still available only after an unknown integration time in the exposure measurement circuit. In addition, mismatch between the outputs of the pixels may be problematic. For example, without a pixel mismatch correction method, direct use of the exposure measurement of a logarithmic photoreceptor circuit is problematic in an array of pixels.

Patent US 9,631,974 discloses a photoarray, comprising a plurality of cells, wherein each of said cells comprises:

- a means that is configured to generate a photocurrent being proportional to the intensity of the light impinging on the respective cell;
- a change detection circuit connected to the respective means for generating the photocurrent, which change detection circuit is configured to generate an output signal merely in case a change event occurs at which said intensity changes by a threshold amount;
- a brightness readout circuit that is configured so as to allow for reading a signal representing the brightness at the respective cell.

However, the photoarray uses conventional frame-based readout of the brightness (grey level) values with fixed exposure time. Brightness readout is not directly triggered by the change detection circuit of the individual pixels but is performed frame-wise from external control just like a conventional image sensor.
Patent US 9,528,738 discloses a pixel cell comprising a light change detector with a high-pass filter. However, mismatch between the outputs of the pixels may be problematic. For example, without a pixel mismatch correction method, direct use of the exposure measurement of a logarithmic photoreceptor circuit is problematic in an array of pixels.

SUMMARY OF THE INVENTION

The invention aims at providing an event-based image sensor with pixel circuits with smaller area requirements, allowing for larger array sizes or smaller sensor chip dimensions. The invention also aims at speeding up the individual measurement processes and consequently increasing temporal resolution. The invention also aims at avoiding spatial divergence between change detection and exposure measurement caused by a use of two separate photodiodes, improving measurement accuracy and consequently image quality. The invention also aims at providing exposure measurements immediately available after detection of a change, individually for each single pixel. The invention also aims at reducing mismatch between pixel circuits.

In this respect, the invention relates to an event-based image sensor comprising a controller, an address-event representation circuitry, and a plurality of pixel circuits forming a pixel array, the controller connected to each pixel circuit to control said pixel circuits, each pixel circuit comprising:

- a photoreceptor circuit comprising a light-sensitive element and having an output, said photoreceptor circuit being configured for delivering at said output a photoreceptor current derived from a light impinging on the light-sensitive element,

- an analog bus selectively connected to a readout unit, the output of the photoreceptor circuit being selectively connected to said analog bus,

- a bank of current memory cells connected to the analog bus, each current memory cell being adapted to selectively store an electric current flowing in the analog bus and to selectively deliver into said analog bus an electric current stored within said current memory cell;

wherein each pixel circuit comprises a current comparator configured for detecting a change in the photoreceptor current, said current comparator comprising:
- a current sign detector connected to the analog bus and configured for determining a sign of a value of an electric current flowing in the analog bus resulting from a compared electric current and a threshold current, said compared electric current resulting from a difference between at least the photoreceptor current and a previous photoreceptor current stored in a current memory cell,

- at least one storage cell connected to an output of the current sign detector and having a state conditioned by the output of said current sign detector, the state of said at least one storage cell being representative of a change between the photoreceptor current and the previous photoreceptor current greater than the threshold current;

wherein said at least one digital storage cell is connected to the address-event representation circuitry so that the address-event representation circuitry monitors the state of the storage cell to determine a change in the light impinging on the light-sensitive element, and

wherein a readout of a pixel circuit through the connection of the analog bus to the readout unit is conditioned by the state of said at least one digital storage cell.

In contrast to prior art event-based image sensor, a pixel circuit here is a simpler circuit, that does not require large capacitors or switched capacitor circuits. In addition, the storage cell is used as a flag to indicate to the address-event representation circuitry that a change in the light has occurred, and the photoreceptor current is immediately available for a readout.

Other preferred, although non-limitative, aspects of the image sensor are as follows, isolated or in a technically feasible combination:

- the current comparator comprises a first storage cell and a second storage cell, each connected to the output of the current sign detector and having a state conditioned by the output of said current sign detector, the state of the first storage cell representative of a value of the compared electric current greater than a value of a first threshold current, the state of the second storage cell representative of a value of the compared electric current lower than a value of a second threshold current;
- the compared electric current is obtained by connecting a current memory cell storing the photoreceptor current and a current memory cell storing the previous photoreceptor to the
analog bus, and storing it into a current memory cell, the threshold current being stored in another current memory cell;
- the address-event representation circuitry is configured to determine an address of the pixel circuit whose digital storage cell has changed state upon detection of a change in a state of a digital storage cell of a pixel circuit;
- the controller is configured for sending instructions to the pixel circuits, and wherein execution of at least one instruction by a pixel circuit is conditioned by a state of at least one storage cell;
- the photoreceptor circuit a pixel circuit is a logarithmic photoreceptor circuit and the photoreceptor current is proportional to a logarithm of the light impinging on the light-sensitive element;
- the event-based image sensor further comprises a calibration current source, and the photoreceptor circuit of a pixel circuit is configured for delivering at the output of said photoreceptor circuit a calibration current derived from a reference calibration current supplied by the calibration current source during a calibration procedure.

The invention also relates to a method of operating an event-based image sensor according to the invention, comprising a change detection cycle for detecting a change in light impinging onto a light-sensitive element of a photoreceptor circuit of a pixel circuit, said change detection cycle comprising the following steps:

a) the photoreceptor circuit delivers a photoreceptor current derived from a light exposure of the light-sensitive element at the output of said photoreceptor circuit and the photoreceptor current is written in a first current memory cell of the memory bank,

b) a compared electric current resulting from a difference between the photoreceptor current and a previous photoreceptor current stored in a second current memory cell is stored in another current memory cell,

c) the current sign detector compares a value of the compared electric current with a value of a threshold current stored in another current memory cell, and if the value of the compared electric current is above the value of the threshold current, the state of a digital storage cell is set in a first state,

d) if the storage cell is in the first state, a readout of the photoreceptor current is performed, the photoreceptor current is written in the second current memory cell, and the state of the storage cell is set to a second state.
Other preferred, although non-limitative, aspects of the method are as follows, isolated or in a technically feasible combination:

- a current comparator of the pixel circuit comprises a first storage cell and a second storage cell, each connected to the output of a current sign detector of the current comparator and having a state conditioned by an output of said current sign detector, the state of the first storage cell representative of a value of the compared electric current greater than a value of a first threshold current, the state of the second storage cell representative of a value of the compared electric current lower than a value of a second threshold current, wherein step c) is composed of the following steps:
  
  c1) the current sign detector compares a value of the compared electric current with a value of a first threshold current stored in a fourth current memory cell, and if the value of the compared electric current is above the value of the first threshold current, the state of the first storage cell is set in a first state,
  
  c2) the current sign detector compares a value of an opposite of the compared electric current with a value of a second threshold current stored in a fifth current memory cell, and if the value of the opposite of the compared electric current is above the value of the second threshold current, the state of the second storage cell is set in a first state;

- during a readout procedure of the pixel array, only pixel circuits that have a storage cell is a first state are selected to have their photoreceptor current read;

- the method comprises a calibration procedure executed before step d) of the detection cycle, said calibration procedure comprising the following steps:
  
  - connection of a calibration current source instead of a light-sensitive element in a photoreceptor circuit of a pixel circuit so that the photoreceptor circuit of the pixel circuit delivers at the output of said photoreceptor circuit a calibration current derived from a reference calibration current supplied by the calibration current source,
  
  - transferring the calibration current from the output of said photoreceptor circuit to a sixth current memory cell where said calibration current is stored;

- during a readout of a pixel circuit, the calibration current stored in the sixth current memory cell is subtracted from the photoreceptor current.
BRIEF DESCRIPTION OF THE DRAWINGS

Other aspects, objects and advantages of the present invention will become better apparent upon reading the following detailed description of preferred embodiments thereof, given as non-limiting examples, and made with reference to the appended drawings wherein:

- figure 1 shows a simplified diagram of an event-based image sensor according to a possible embodiment of the invention;
- figure 2 shows a simplified diagram of a pixel circuit according to a possible embodiment of the invention;
- figures 3 shows a simplified diagram of an exemplary possible embodiment of a photoreceptor circuit;
- figure 4 shows a simplified diagram of an exemplary possible embodiment of a memory cell;
- figure 5 and 6 show diagrams of a method of operating a pixel circuit according to a possible embodiment of the invention.

In all figures, the same reference characters refer to same or similar elements.

DETAILED DESCRIPTION OF THE INVENTION

A simplified diagram of an event-based image sensor according to a possible embodiment is shown in figure 1. The event-based image sensor comprises a plurality of pixel circuits 1 forming a pixel array. Figure 1 shows a limited number of pixel circuits 1 for clarity's sake. It is understood that the pixel array comprises a large number of pixel circuits 1, with dimensions exceeding 256 x 256 pixels for example. The event-based image sensor comprises a controller 2, an address-event representation (AER) circuitry 3 and may also comprise a calibration current source 4.

The controller 2 is configured for sending instructions to the pixel circuits 1 in order to control the pixel circuits 1. According, the pixel circuits are connected to the controller 2. The controller 2 is configured to send the same instruction at the same time to all the pixel circuits 1. The controller 2 and the pixel circuits 1 form a single instruction, multiple data (SIMD) processing architecture.
An example of a pixel circuit is illustrated on figure 2. A pixel circuit comprises a photoreceptor circuit having an output and configured for delivering at said output a photoreceptor current. The photoreceptor current is derived from light impinging a light-sensitive element of the photoreceptor circuit.

Figure 3 shows an example of a photoreceptor circuit that may be used. The photoreceptor circuit is a logarithmic photoreceptor circuit, and the photoreceptor current \( I_{\text{PrOut}} \) is proportional to a logarithm of the light impinging on the light-sensitive element 101. The photoreceptor circuit comprises a light-sensitive element 101 such as a photodiode, which is connected to ground and via a switch \( S_2 \) to an input 102 of an inverting amplifier 103. A N-type MOSFET transistor 104 has its drain connected to a supply voltage terminal 110, and its source connected to the input 102 of the inverting amplifier 103. The output 105 of the inverting amplifier 103 is connected to the gate of the transistor 104. The inverting amplifier 103 delivers at its output 105 a photoreceptor voltage \( V_{\text{Pr}} \) derived from the light exposure of the light-sensitive element 101. The output of the inverting amplifier 103 is also connected to the input of a voltage-to-current (V/I) converter 106 that converts the photoreceptor voltage \( V_{\text{Pr}} \) into the photoreceptor current \( I_{\text{PrOut}} \) that is delivered on the output 11 of the photoreceptor circuit 11 constituted by the output of the voltage-to-current converter 106. The calibration source 4 can be connected to the input 102 through a switch \( S_1 \) for delivering a reference current \( I_{\text{Ref}} \) to the input 102.

Other kinds of photoreceptor circuit may be used. For example, the photoreceptor circuit 10 may be a linear photoreceptor circuit which delivers a current linearly proportional to the light impinging on the light-sensitive element 101. Preferably, the photoreceptor current \( I_{\text{PrOut}} \) may also be a current derived from a voltage at a capacitor resulting from an integration over a given amount of time of the current flowing through the light-sensitive element 101, as described in the prior art references cited above. It is also possible to combine in a same pixel circuit a logarithmic photoreceptor circuit with another photoreceptor circuit provided with an integrating capacitor.

The pixel circuit also comprises an analog bus 20 wherein electric currents can flow. The output 11 of the photoreceptor circuit 10 is connected to said analog bus 20 through a front-end switch \( S_{\text{Pr}} \). The analog bus 20 is connected to a current readout unit. More precisely, a readout switch \( S_{\text{R}} \) connects analog bus 20 to said current readout unit. The switch \( S_{\text{R}} \) is closed when the pixel circuit is selected to be read. The current readout unit is for example a column current readout unit. The current readout unit may include a current-
to-voltage converter block to which the electric current flowing in the analog bus of a
selected pixel circuit is routed, and an analog-to-digital converter (ADC).

The pixel circuit 1 also comprises a bank of memory cells IS; (with i=1…6) connected to the bus. In the depicted embodiment, the bank of memory cells IS; comprises six memory cells IS;: However, the number of memory cells IS; in the bank may vary. The number of memory cells IS; is preferably greater than or equal to four, and more preferably greater than or equal to five, and even more preferably greater than or equal to six. Each memory cell IS; is adapted to selectively store an electric current flowing in the analog bus 20 and to selectively deliver into said analog bus 20 an electric current stored within said memory cell IS;.

Figure 4 shows a schematic example of a current memory cell IS; that can be used in a pixel circuit 1. The memory cell IS; comprises an N-type field-effect transistor 40 (e.g. MOSFET), with a source at ground. A capacitor 41 has a first terminal connected to the ground and a second terminal connected to the gate of the transistor 40. Accordingly, the voltage $V_{GS}$ across the capacitor 40 corresponds to the voltage between the gate and the source of the transistor 40. The second terminal of the capacitor 41 is also connected to the drain of the transistor 40 through a gate switch $S_G$. The drain of the transistor 40 is connected to the analog bus 20 through a drain switch $S_D$. When the drain switch $S_D$ is closed, the memory cell IS; is connected to the analog bus 20. A current source 42 is connected to the drain of the transistor 40 and allows a reference current $I_{ref}$ to flow in both directions. The current source 42 may be outside the memory cell ISi, and may be shared by the memory cells ISi of the bank of a pixel circuit, or by the memory cells ISi of the whole pixel array. Other types of current memory cell ISi can be used. For instance, the article of J. B. Hughes and K. W. Moulding "S2I: A switched-current technique for high performance", Electron. Fett., vol. 29, no. 16, pp. 1400-1401, Aug. 1993.

When the drain switch $S_D$ and the gate switch $S_G$ are closed, the voltage $V_{GS}$ takes the value required for an electric current to flow flowing from the analog bus 20 through the transistor 40. The incoming electric current is thereby written in the memory cell ISi. When the drain switch $S_D$ and the gate switch $S_G$ are open, the voltage $V_{GS}$ keeps a constant value. The electric current is stored in the memory cell ISi. When the gate switch $S_G$ is open and the drain switch $S_D$ is closed, the voltage $V_{GS}$ at the gate of the transistor 40 is kept (because the gate switch $S_G$ is open), but the electric current flows (because of the
voltage $V_{GS}$ at the gate of the transistor 40) to the analog bus 20. The electric current is read from the memory cell IS;.

Since the pixel circuit 1 comprises several current memory cells IS; connected to the same analog bus 20, it is possible to perform arithmetic operations on electric currents, by writing, storing and reading said electric currents. Furthermore, electric currents can be inverted and copied from one current memory cell IS; to another current memory cell IS;:

The results of these arithmetic operations are also electric currents that can be stored in the current memory cells IS;. These operations simply follow Kirchoff’s current law.

For example, to perform an addition of two electric currents respectively stored in two memory cells, said two memory cells just have to be connected to the analog bus 20 and read at the same time (i.e. by closing the drain switches $S_D$ and keeping the gate switch $S_G$ open). The resulting current may be written in another current memory cell at the same time (by opening both the drain switches $S_D$ and the gate switch $S_G$).

It shall be noted that when a current memory cell IS; is read from and another current memory cell IS; is writing, the electric current from the read current memory cell and entering the analog bus 20 is the opposite of the electric current leaving the analog bus 20 to be written, according to Kirchoff’s current law. As a consequence, for the analog bus 20, a basic transfer operation between two current memory cells IS; includes a negation of the value of the transferred electric current (i.e. of the intensity of the transferred electric current). As a consequence, it is possible to substrate a value of a first electric current from a value of a second electric current by transferring first electric current from one current memory cell to another current memory cell before adding the two electric currents.

The pixel circuit 1 also comprises a current comparator 50 configured for detecting a change in the photoreceptor current $I_{Phot}$. The current comparator 50 comprises a current sign detector 51 with an input connected to the analog bus 20 by a comparator switch $s_{comp}$. The current sign detector 51 is configured to determine the sign of the value of the electric current (i.e. the direction of the current) flowing in the analog bus 20. Preferably, the current sign detector 51 is configured to output a value only when the current at its input (i.e. through the comparator switch $s_{comp}$) is positive.

The current comparator 50 also comprises two storage cells 53, 54 connected to the output 52 of the current sign detector 51. A first storage cell 53 is connected through a first flag switch $S_A$ and constitutes a first flag A. A second storage cell 54 is connected through a second flag switch $S_B$ and constitutes a second flag B. The storage cells 53, 54 can have
two states, a first state designated as "TRUE", and a second state designated as "FALSE". The default state of a storage cell 53, 54 is "FALSE". A storage cells 53, 54 keeps its state until said storage cell 53, 54 is reset. A reset signal rst can be provided to the storage cells 53, 54 to force them into the second state (i.e. FALSE). The storage cells 53, 54 can therefore be considered as latches. The storage cells 53, 54 can also be called digital storage cell because they can only have two states that can be construed as binary values.

The two digital storage cells 53, 54 are connected to the address-event representation circuitry 3. The address-event representation circuitry 3 monitors the states of the digital storage cells 53, 54 of all the pixel circuits 1.

In reference to figures 5 and 6, a detection cycle of a pixel circuit 1 is described herein below. Figures 5 and 6 show different aspect of the same cycle: figure 5 shows how the electric current are used, and figure 6 shows how the switches and current memory cells IS; are used. In the steps of the following description, when a memory cell IS; is in writing mode, the drain switch SD and the gate switch SG of said memory cell IS; are closed. When a memory cell IS; is in reading mode, the drain switch SD of said memory cell IS; is closed while the gate switches SG is kept open. When a memory cell IS; is in an idle mode, i.e. neither in writing mode nor in reading mode, the drain switch SD and the gate switch SG are open. A memory cell IS; in idle mode is disconnected from the analog bus 20 and stores an electric current. If a current memory cell IS; is not mentioned during a step, the current memory cell IS; should be considered in idle mode. Unless mentioned otherwise, the switches and therefore the operations of the steps of the change detection cycle are controlled by the instructions sent by the controller 2. The same instruction is sent at the same time to all the pixel circuits 1 by the controller 2.

In a first step S0I, the photoreceptor circuit 10 delivers a photoreceptor current IPROUT derived from a light exposure of the light-sensitive element 101 at the output 11 of said photoreceptor circuit 10, and the photoreceptor current IPROUT; is written in a first current memory cell IS;i of the memory bank. More precisely, the front-end switch SPR is closed (step SII), connecting the output 11 of the photoreceptor circuit 10 to the analog bus 20. The photoreceptor current IPROUT therefore flows into the analog bus 20. The first current memory cell IS;i is in writing mode so that the photoreceptor current IPROUT; is written in the first current memory cell IS;i. The front-end switch SPR is then opened.

In step S02, a previous photoreceptor current IPROUT; last stored in a second current memory cell IS;2 is substracted from the photoreceptor current IPROUT; stored in the first
current memory cell ISi, resulting in a compared electric current which is stored in a third current memory cell IS3. More precisely, the first current memory cell ISi and the second current memory cell IS2 are in reading mode and the third current memory cell IS3 is in writing mode (step S12). Since a reading a memory cell ISi after writing an electric current in said memory cell ISi reverses the flowing direction of the electric current on the analog bus 20, it reverses the sign of the value of the electric current. As a result, the electric current read from the first current memory cell ISi has a value of -IpR_out. By reading the first current memory cell ISi and the second current memory cell IS2 at the same time, the compared electric current written in the third current memory cell IS3 has a value of -IpR_out + IpRout, last.

In step S03, the current sign detector S1 compares a value of the first compared electric current with a value of a first threshold current stored in a fourth current memory cell IS4. The state of the first digital storage cell 53 will depend from the result of the comparison. To do so (step S13), the third current memory cell IS3 and the fourth current memory cell IS4 are in reading mode in order to send to the analog bus 20 the first compared electric current of value -(IpR_out + IpRout, last), noted I_compared, and the first threshold current, respectively. For instance, if the photoreceptor current has a value of IpRout = 1.1 μA, and the previous photoreceptor current has a value of IpR_out, last = 1 μA, the compared electric current has a value of I_compared = 0.1 μA. It shall be noted that the example of current values are given here and below as a mere illustration and may not reflect the actual current values used in embodiments of the invention.

The resulting electric current on the analog bus 20 therefore shows a value of I_compared + f_thA, where I_tha is the value of the first threshold current. The comparator switch S_comp is closed in order to connect the current sign detector S1 to the analog bus 20. The first flag switch SA is also closed to connect the first storage cell 53 to the output 52 of the current sign detector S1. For comparing the value of the compared electric current I_compared flowing in the analog bus 20 with the value of the first threshold current I_thA, the current sign detector S1 is configured to determine a sign of the current (i.e. sign of the intensity or value of the current) of the resulting electric current flowing in the analog bus 20. If the value of the resulting electric current is positive, I_compared + I_thA is positive, which means that the value of the first compared electric current I_compared is greater than the opposite of the value of the first threshold current I_thA. This means that a positive change between the photoreceptor current and the previous photoreceptor current is greater than the opposite of
the first threshold current, and therefore that the light impinging on the light-sensitive
element 101 has increased since a previous change detection cycle. This change is thus
detected. For example, if \( I_{\text{th}} = -0.1 \, \mu\text{A} \), so \( I_{\text{compared}} + I_{\text{th}} = 0.01 \, \mu\text{A} \), which is positive.
Indeed, the photoreceptor current of 1,1 \( \mu\text{A} \) exceeds the previous photoreceptor current of
\( 1 \, \mu\text{A} \) by more than the opposite value of the first threshold current of -0.1 \( \mu\text{A} \).

Conversely, if the value of the resulting electric current has a negative sign, this
means that the light impinging on the light-sensitive element 101 has not increased enough
with respect to a previous change detection cycle to justify detecting a change, or has
decreased.

The current sign detector 51 outputs the result of the comparison on its output 52.
The state of the digital storage cell 53 is changed or not depending on the result of the
comparison: if a change greater than the first threshold current is detected, the state of the
first storage cell 53 is changed to a first state, i.e. to TRUE; conversely if no change greater
than the first threshold current is detected, the state of the digital storage cell 53 is
unchanged and kept in a second, default state, i.e. FALSE state. The first flag switch \( S_A \)
is then opened to keep the state of the first storage cell 53.

In step S04, the photoreceptor current \( I_{\text{P0U}} \) is subtracted from the previous
photoreceptor current \( I_{\text{P0U,t, last}} \). This is the opposite of step S02. Since the compared
electric current \( I_{\text{compared}} \) corresponding to the difference between photoreceptor current
\( I_{\text{P0U}} \) and the previous photoreceptor current \( I_{\text{P0U,t, last}} \) is already stored in the third current
memory cell IS3, this compared electric current \( I_{\text{compared}} \) just have to be written in another
memory cell, e.g. the first current memory cell IS1, to change the sign of its value.
Accordingly, in step S14, the third current memory cell IS3 is in reading mode while the
first current memory cell IS1 is in writing mode. The compared electric current \( I_{\text{compared}} \)
propagates through the analog bus 20 from the third current memory cell IS3 to the first
current memory cell IS1, changing the sign of its value. It would also be possible to
retrieve the photoreceptor current from the photoreceptor circuit 1 and the previous
photoreceptor current \( I_{\text{P0U,t, last}} \) from the second current memory cell IS2.

In step S05, the current sign detector 51 compares the value of the compared
electric current with a value of a second threshold current stored in a fifth current memory
cell IS5. The state of the second digital storage cell 54 will depend from the result of the
comparison. To do so, the first current memory cell IS1 and the fifth current memory cell
IS5 are in reading mode in order to send to the analog bus 20 the compared electric current
of value \(-I_{pR} \alpha_{1} + I_{pRout}\), last, noted \(-I_{compared}\), and the second threshold current of value \(I_{thB}\), respectively. The resulting electric current on the analog bus 20 therefore shows a value of \(I_{thB} - I_{compared}\). The comparator switch \(S_{comp}\) is closed to connect the current sign detector 51 to the analog bus 20. The second flag switch \(S_{B}\) is also closed to connect the second storage cell 54 to the output 52 of the current sign detector 51. If the value of the resulting electric current is positive, \(I_{thB} - I_{compared}\) is positive, which means that the value of the compared electric current \(I_{compared}\) is lower than the value of the second threshold current \(I_{thB}\). This means that a negative change between the photoreceptor current and the previous photoreceptor current is greater than the second threshold current, and therefore that the light impinging on the light-sensitive element 101 has decreased enough since a previous change detection cycle. This change is thus detected.

Conversely, if the value of the resulting electric current is negative, it means that the light impinging on the light-sensitive element 101 has not decreased enough with respect to a previous change detection cycle to justify detecting a change, or has increased.

For example, with \(I_{compared} = 0.1\ \mu A\) and \(I_{thB} = -0.1\ \mu A\), \(I_{thB} - I_{compared} = -0.21\ \mu A\). The resulting electric current is negative, because the photoreceptor current of 1.1 \(\mu A\) is not lower than the previous photoreceptor current of 1 \(\mu A\) by more than the opposite value of the second threshold current of -0.1 \(\mu A\).

The current sign detector 51 outputs the result of the comparison on its output 52. The state of the second digital storage cell 54 is changed or not depending on the result of the comparison: if a negative change greater than the second threshold current is detected, the state of the second digital storage cell 54 is changed to a first state, i.e. to TRUE; conversely if no negative change greater than the first threshold current is detected, the state of the second digital storage cell 54 is unchanged and kept in a second, default state, i.e. FALSE state. The second flag switch \(S_{B}\) is then opened to keep the state of the second digital storage cell 54.

It shall be noted that the order in which are used the threshold current here is purely illustrative, and that steps S02 and S03 may be performed after steps S04 and S05 if desired. In the numerical example, the threshold currents have the same values, and therefore the first threshold current and the second threshold may be one single threshold current. However, the first threshold current and the second threshold current may have different values, in order to detect differently positive or negative changes. Preferably, the first threshold current and the second threshold current have negative values, because
photoreceptor current is positive. However, since it is easy to change the signs of an
electric current by using a current memory cell, the skill person would understand that the
signs of the currents mentioned in that description may be easily changed individually for
each current.

Resulting from steps S03 and S05, the states of the flags A and B have been
determined. The address-event representation (AER) circuitry 3 monitors the state of the
flags A and B. If one of the storage cells 53, 54 of a pixel circuit 1 turns to TRUE, the AER
circuitry 3 can, if other external conditions are met, execute the construction of the array
address (i.e. x,y array address) of that particular pixel circuit 1. This address and the
information about which flag (A or B) is TRUE can be sent by the AER circuitry 3 to an
address readout system. The external conditions may for example depend on the state of
the AER circuitry 3, on the result of an external computation or of a measurement.

Readout of the pixel circuit 1 firstly comprises an exposure measurement. Step S06
is the measurement of the photoreceptor current $I_{\text{phot}}$ to determine the exposure
measurement of the light-sensitive element 101. It is conditioned by the states of the storage
cells 53, 54. The exposure measurement instruction is sent by the controller 2 to all
the pixel circuits 1, but only the pixel circuits 1 with a digital storage 53, 54 in a TRUE
state execute this readout instruction. Pixel circuits 1 with a digital storage 53, 54 in a
TRUE state will be designated as active pixel circuits 1. Execution of the exposure
measurement instruction may be further conditioned by other conditions, summarized as a
global condition "EM enabled" in figures 5 and 6.

Preferably, an in-pixel calibrated exposure measurement is performed by an active
pixel circuit 1. A calibration current is subtracted from the photoreceptor current $I_{\text{phot}}$, and
the resulting current is sent to a current readout unit through the analog bus 20. The
calibration current is stored in a sixth current memory cell IS6. Storage of the calibration
current in the sixth current memory cell IS6 is done during a calibration procedure that can
be executed at any time, for example at the beginning of the change detection cycle or
previously. Preferably, the calibration procedure is performed by all the pixel circuits 1 at
the same time upon instruction from the controller 2.

During a calibration procedure, the switch S2 between the light-sensitive element
101 and the input 102 of the inverting amplifier 103 is opened. The switch S1 of the
photoreceptor circuit 10 is closed so that the calibration source 4 is connected to the input
102 instead of the light-sensitive element 101. The calibration source 4 delivers an external
reference calibration current $I_{cal}$ to the input 102 which is also the source of the transistor 104. Consequently, the electric current at the output 11 of the photoreceptor circuit 10 is a calibration current $I_{cal,0}$. The front-end switch SPR is closed in order to connect the output 11 to the analog bus 20. The sixth current memory cell IS6 is in writing mode, and stores the calibration current $I_{cal,0}$. At the end of the calibration procedure, the switch S1 is reopened and the switch S2 is closed, thus reverting the photoreceptor circuit 10 to its normal configuration.

Since the external reference calibration current $I_{cal}$ travels the same path as the photoreceptor current $I_{cal,0}$ to become the stored calibration current $I_{cal,0}$, the stored calibration current $I_{cal,0}$ of a pixel circuit reflects the variations of the electrical characteristics of that particular pixel circuit 1 that could impact the photoreceptor current $I_{cal,0}$. As a result, the calibration current $I_{cal,0}$ of a pixel circuit is unique and specific to each pixel circuit since the properties of the components of a pixel circuit vary from one pixel circuit to another pixel circuit, in particular because of the photoreceptor circuits. This is called device mismatch. Subtracting the calibration current $I_{cal,0}$ from the photoreceptor current $I_{cal,0}$ allows removing the effects of device mismatch from the exposure measurement results. In particular, with a logarithmic photoreceptor as the one depicted in figure 4, the exposure measurement results may suffer from large errors due to device mismatch, amplified by the logarithmic nature of the response.

There is no need for writing a new calibration current for each change detection cycle or readout, and a same calibration current may be used during several change detection cycles or exposure measurements. The calibration current stored in the sixth current memory cell IS6 is however preferably updated frequently enough to reflect the variation of the factors influencing the pixel circuit (temperatures, interferences, etc.).

For performing the calibrated exposure measurement, the sixth current memory cell IS6 is in reading mode and the front-end switch SPR is closed, so that the resulting current in the analog bus 20 is the readout current $I_{cal,0} - I_{cal,0}$ (step S16). When the readout switch $S_{read}$ is closed, the analog bus 20 is connected to the current readout unit, and the readout current is sent to said current readout unit, through an Current-to-voltage (I/V) converter and/or an analog-to-digital converter (ADC). The pixel circuit 1 is thus read.

At least the closure of the readout switch $S_{read}$ is not performed by all the active pixel circuits 1 at the same time. The active pixel circuits 1 are sequentially selected to be read. Active rows, i.e. rows with at least one active pixel circuit 1, are for example first selected.
The active rows may be selected by scanning each row to detect the presence of an active pixel circuit 1 or directly selected by an AER arbiter of the AER circuitry 3 based on the addresses of the active pixel circuits 1 determined through the monitoring of the states of the flags A and B.

For each selected row, each active pixel circuit 1 is then read by closing the readout switch $S_o$. This can be done on a column-by-column basis (i.e. active column that have at least one active pixel circuit 1) or in parallel for all active rows if a column reader is provided (in particular with a column I/V converter and/or a column ADC). Alternatively, with a column-wise readout, all active pixel circuits 1 per row may be read in parallel.

If a first approach, all the active pixel circuits 1 of the image sensor are read before resuming or restarting the change detection cycle. This results in a non-uniform "frame rate" in the sense that the duration of the readout procedure, and further the duration of the change detection cycle, depends on the number of active pixel circuits 1, i.e. the number of pixel circuits 1 that detected a change and set their flags to TRUE. Accordingly, the frame rate depends on the activity of the scene acquired by the event-based image sensor, i.e. how the light changes.

In a second approach, all the active pixel circuits 1 are not necessarily read before resuming or restarting the change detection cycle. The change detection cycle may be restated or resumed before every active pixel circuits 1 have been read, for example after a certain amount of time has passed or after a certain amount of pixel circuits 1 have been read. The amount of time allocated to the readout may be fixed (i.e. fixed "frame-rate"), or may varies. Similarly, the number of active pixel circuits 1 that have been read may be fixed (i.e. fixed "frame-rate"), or may varies.

It is also possible to combine the two approaches, for example by resuming or restarting the change detection cycle either when all the active pixel circuits 1 have been read or when a certain amount of time has passed (a certain amount of pixel circuits 1 have been read) if there are too many pixel circuits to read.

In step S07, if one of the flags of the pixel circuit 1 is set at TRUE, i.e. if one of the storage cell 53, 54 is in the first state, the photoreceptor current $I_{R0Ut}$ replaces the previous photoreceptor current $I_{R0Ut}_{last}$ to be used as a new previous photoreceptor current for a new change detection cycle. To do so, the photoreceptor current $I_{R0Ut}$ is written in the second current memory cell IS2.
To avoid changing the sign of the value of the photoreceptor current $I_{pR\_1\_t}$, the photoreceptor current $I_{pR\_1\_t}$ is firstly written in another memory cell. For example, in step $s_{17}$ the front-end switch $SPR$ is closed to connect the output $1\_1$ of the photoreceptor circuit 10 to the analog bus 20 to make the photoreceptor current $I_{pR\_1\_t}$ available on the analog bus 20. The first current memory cell IS1 is in writing mode and writes the photoreceptor current $I_{pR\_1\_t}$. The front-end switch $SPR$ is then opened, and the first current memory cell IS1 enters reading mode while the second current memory cell IS2 enters writing mode. The photoreceptor current $I_{pR\_1\_t}$ is transferred from the first current memory cell IS1 into the second current memory cell IS2. By doing so, the sign of the value of the photoreceptor current $I_{pR\_1\_t}$ would be changed twice when read again. The electric current stored in the second current memory cell IS2 will be used as the previous photoreceptor current $I_{pR\_1\_t\_last}$ during the next change detection cycle of the pixel circuit 1.

Rather than expressly using the photoreceptor circuit 10 again to get the photoreceptor current $I_{pR\_1\_t}$, it is possible to use electric currents already stored in current memory cells. For example, the compared electric current $I_{compared}$ and its opposite $-I_{compared}$ stored in the first current memory cell IS1 and in the third current memory cell IS3 can be used to retrieve the photoreceptor current $I_{pR\_1\_t}$ because they correspond to $\pm (I_{pR\_1\_t} - I_{pRout\_last})$. The photoreceptor current $I_{pRout\_last}$ may also be stored during the exposure measurement in a current memory cell that is no longer of use in that change detection cycle such as the first current memory cell IS1 or the third current memory cell IS3.

Finally, in step $s_{58}$ at the end of the change detection cycle, the flags are cleared, i.e. reset to the default state FALSE. A reset signal $rst$ is sent (step $s_{18}$) to the storage cells 53, 54 to force them into the second state (i.e. False). If all the active pixel circuits 1 were read, all the flags can be cleared and the reset signal $rst$ can be sent by the controller 2 to all the pixel circuits 1.

However, if some active pixel circuits 1 were not read during the readout procedure, for example because the time allocated to do so has elapsed, it is preferable not to clear the flags of unread active pixel circuits 1. Accordingly, the reset signal $rst$ can be selectively sent to each pixel circuit 1 that is read during the readout procedure. Unread active pixel circuits 1 therefore stay active, i.e. with their flags in the state TRUE, and will be read during the next readout procedure. Preferably, active pixel circuits 1 are not read in the same order during subsequent readout procedures, so that the active pixel circuits 1 that
were not read a readout procedure will be the first ones to be read during the next readout procedure.

Similarly, step S07 is preferably not performed by the active pixel circuits 1 that were not read during the readout procedure, but performed only by active pixel circuits that were read during readout procedure. This can be done by performing step S07 as part of the readout procedure.

In the change detection cycle described herein above, the current comparator 50 comprises two storage cells 53, 54: the state of the first storage cell 53 representative of an increase in the value of the photoreceptor current, the state of the second storage cell 54 representative of a decrease in the value of the photoreceptor current. Accordingly, the AER circuitry 3 may determine through the monitoring of the state of the storage cells 53, 54 how the photoreceptor current has changed: with an increase event or a decrease event (no event means no change). However, it is possible to have only one storage cell connected to the current sign detector 51. In this case, the AER circuitry 3 could only determine that a change has occurred in the photoreceptor current of a pixel circuit 1. This may be sufficient since the detection of a change is mainly used for determining the address of the pixel circuit 1 and for conditioning the readout of the pixel circuit 1. In the operating method, a second comparison between a value of a compared electric current flowing in the analog bus with a value of a threshold current could be conditioned by the state of the unique flag. Indeed, if the state of the flag has been changed in the first comparison, there is no need to do the second comparison. It is also possible to have a second comparison conditioned by the state of the first storage cell 53 in the case with two storage cells 53, 54.

While the present invention has been described with respect to certain preferred embodiments, it is obvious that it is in no way limited thereto and it comprises all the technical equivalents of the means described and their combinations. In particular, it will be apparent to those skilled in the art that various changes and modifications may be made without departing from the scope of the invention as defined in the appended claims.
Claims

1. An event-based image sensor comprising a controller (2), an address-event representation circuitry (3), and a plurality of pixel circuits (1) forming a pixel array, the controller (2) connected to each pixel circuit (1) to control said pixel circuits (1), each pixel circuit (1) comprising:
   - a photoreceptor circuit (10) comprising a light-sensitive element (101) and having an output (11), said photoreceptor circuit (10) being configured for delivering at said output (11) a photoreceptor current (Ip_Rout) derived from a light impinging on the light-sensitive element (101),
   - an analog bus (20) selectively connected to a readout unit, the output (11) of the photoreceptor circuit (10) being selectively connected to said analog bus (20),
   - a bank of current memory cells connected to the analog bus (20), each current memory cell (ISi) being adapted to selectively store an electric current flowing in the analog bus (20) and to selectively deliver into said analog bus (20) an electric current stored within said current memory cell (ISi);

wherein each pixel circuit (1) comprises a current comparator (50) configured for detecting a change in the photoreceptor current (Ip_Rout), said current comparator (50) comprising:
   - a current sign detector (51) connected to the analog bus (20) and configured for determining a sign of a value of an electric current flowing in the analog bus (20) resulting from a compared electric current and a threshold current, said compared electric current resulting from a difference between at least the photoreceptor current and a previous photoreceptor current stored in a current memory cell,
   - at least one storage cell (53, 54) connected to an output (52) of the current sign detector (51) and having a state conditioned by the output of said current sign detector (51), the state of said at least one storage cell (53, 54) being representative of a change between the photoreceptor current and the previous photoreceptor current greater than the threshold current;

wherein said at least one digital storage cell (53, 54) is connected to the address-event representation circuitry (3) so that the address-event representation circuitry (3) monitors the state of the storage cell (53, 54) to determine a change in the light impinging on the light-sensitive element (101), and
wherein a readout of a pixel circuit through the connection of the analog bus (20) to the readout unit is conditioned by the state of said at least one digital storage cell (53, 54).

2. The event-based image sensor of claim 1, wherein the current comparator (50) comprises a first storage cell (53) and a second storage cell (54), each connected to the output (52) of the current sign detector (51) and having a state conditioned by the output (52) of said current sign detector (51), the state of the first storage cell (53) representative of a value of the compared electric current greater than a value of a first threshold current, the state of the second storage cell (54) representative of a value of the compared electric current lower than a value of a second threshold current.

3. The event-based image sensor of any one of claims 1 or 2, wherein the compared electric current is obtained by connecting a current memory cell (IS1) storing the photoreceptor current and a current memory cell (IS2) storing the previous photoreceptor to the analog bus (20), and storing it into a current memory cell, the threshold current being stored in another current memory cell.

4. The event-based image sensor of any one of claims 1 to 3, wherein the address-event representation circuitry (3) is configured to determine, upon detection of a change in a state of a digital storage cell (53, 54) of a pixel circuit (1), an address of the pixel circuit (1) whose digital storage cell has changed state.

5. The event-based image sensor of any one of claims 1 to 4, wherein the controller (2) is configured for sending instructions to the pixel circuits (1), and wherein execution of at least one instruction by a pixel circuit (1) is conditioned by a state of at least one storage cell (53, 54).

6. The event-based image sensor of any one of claims 1 to 5, wherein the photoreceptor circuit (10) a pixel circuit (1) is a logarithmic photoreceptor circuit and the photoreceptor current is proportional to a logarithm of the light impinging on the light-sensitive element (101).
7. The event-based image sensor of any one of claims 1 to 6, further comprising a calibration current source (4), and the photoreceptor circuit (10) of a pixel circuit (1) is configured for delivering at the output (11) of said photoreceptor circuit (10) a calibration current derived from a reference calibration current supplied by the calibration current source (4) during a calibration procedure.

8. A method of operating an event-based image sensor according to any one of claims 1 to 7, comprising a change detection cycle for detecting a change in light impinging onto a light-sensitive element (101) of a photoreceptor circuit (10) of a pixel circuit (1), said change detection cycle comprising the following steps:

a) the photoreceptor circuit (1) delivers a photoreceptor current (IpR_out) derived from a light exposure of the light-sensitive element (101) at the output (11) of said photoreceptor circuit (10) and the photoreceptor current (IpR_out) is written in a first current memory cell (IS1) of the memory bank (S01),

b) a compared electric current resulting from a difference between the photoreceptor current and a previous photoreceptor current stored in a second current memory cell (IS2) is stored (S02) in another current memory cell,

c) the current sign detector (51) compares a value of the compared electric current with a value of a threshold current stored in another current memory cell, and if the value of the compared electric current is above the value of the threshold current, the state of a digital storage cell is set in a first state (S03),

d) if the storage cell (53, 54) is in the first state, a readout of the photoreceptor current is performed (S06), the photoreceptor current is written in the second current memory cell (IS2) (S07), and the state of the storage cell (53, 54) is set to a second state (S08).

9. The method of claim 8, wherein a current comparator (50) of the pixel circuit (1) comprises a first storage cell (53) and a second storage cell (54), each connected to the output (52) of a current sign detector (51) of the current comparator (50) and having a state conditioned by an output (52) of said current sign detector (51), the state of the first storage cell (53) representative of a value of the compared electric current greater than a value of a first threshold current, the state of the second storage cell (54) representative of a value of
the compared electric current lower than a value of a second threshold current, wherein step c) is composed of the following steps:

cl) the current sign detector (51) compares a value of the compared electric current with a value of a first threshold current stored in a fourth current memory cell (IS4), and if the value of the compared electric current is above the value of the first threshold current, the state of the first storage cell (53) is set in a first state,

c2) the current sign detector (51) compares a value of an opposite of the compared electric current with a value of a second threshold current stored in a fifth current memory cell (IS5), and if the value of the opposite of the compared electric current is above the value of the second threshold current, the state of the second storage cell (54) is set in a first state.

10. The method of any one of claims 8 to 9, wherein during a readout procedure of the pixel array, only pixel circuits (1) that have a storage cell (53, 54) is a first state are selected to have their photoreceptor current read.

11. The method of any one of claims 8 to 10, comprising a calibration procedure executed before step d) of the detection cycle, said calibration procedure comprising the following steps:

- connection of a calibration current source (4) instead of a light-sensitive element (101) in a photoreceptor circuit (10) of a pixel circuit (1) so that the photoreceptor circuit (10) of the pixel circuit (1) delivers at the output (11) of said photoreceptor circuit (10) a calibration current derived from a reference calibration current supplied by the calibration current source (4),

- transferring the calibration current from the output (11) of said photoreceptor circuit (10) to a sixth current memory cell (IS6) where said calibration current is stored.

12. The method of claim 11, wherein during a readout of a pixel circuit (1), the calibration current stored in the sixth current memory cell (IS6) is substracted from the photoreceptor current.
FIG 1

Controller

AER circuitry

Calibration current source
FIG 5

Storing $I_{PRout}$

Subtracting $I_{PRout, last}$ from $I_{PRout}$

If resulting current is larger than a first threshold
Set Flag A = TRUE

Subtracting $I_{PRout, curr}$ from $I_{PRout, last}$

If resulting current is larger than a second threshold
Set Flag B = TRUE

If Flag A or Flag B = TRUE and EM enabled: do EM readout

Flag A or Flag B = TRUE:
Store $I_{PRout, curr}$ as $I_{PRout, last}$

Clear Flag
(set Flag = False)
FIG 6

S_{PR} closed and IS1 writing

IS1 reading, IS2 reading, IS3 writing

IS3 reading, IS4 reading, S_{comp} and S_{A} closed

IS3 reading, IS1 writing

IS1 reading, IS5 reading, S_{comp} and S_{B} closed

If Flag A or Flag B = TRUE and EM enabled: IS6 reading, S_{PR} closed, S_{ro} closed

Flag A or Flag B = TRUE: S_{PR} closed and IS1 writing, then IS1 reading and IS2 writing

Reset signal srt is sent
INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER

H04N5/335  H04N5/378  H04N5/3745  H04N5/341

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO - Interna l, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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<td>JP H07 203319 A (OLYMPUS OPTICAL CO) 4 August 1995 (1995-08-04) figures 1, 8</td>
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